In the Claims:

Please amend the claims as follows:

1. (original) A Programmable Logic Device (PLD) incorporating a plurality of Programmable Logic Blocks (PLBs) providing enhanced flexibility for Cascade logic functions, each comprising:

- a multi-input Look Up Table (LUT) providing one input to a Cascade Logic block for implementing desired Cascade Logic functions receiving a Cascade-In input as the other input, and
- a 2-input selection multiplexer receiving one input from the output of the Cascade Logic block and the other from the output of the LUT for selecting either the Cascade Logic output or the LUT output as the unregistered output,

the arrangement being such that the output of the cascade logic and the unregistered output are simultaneously available, as separate outputs of the PLB.

2. (currently amended) The [[A]] Programmable Logic Device (PLD) as claimed in claim 1, further including a 2-input Cascade input multiplexer for selecting the Cascade-In signal in either its inverted or non-inverted form as one input to the Cascade Logic.

3. (currently amended) The [[A]] Programmable Logic Device (PLD) as claimed in claim 1, wherein the PLB includes:

- a flip flop connected to the output of the selection multiplexer for providing registered output, and
- a 2-input output multiplexer for selecting either the unregistered output or the registered output as the final output of the PLB

4. (currently amended) The [[A]] Programmable Logic Device (PLD) as claimed in claim 1 wherein the PLB includes a feedback arrangement for connecting the final output to the input of the LUT to enhance the flexibility of the Cascade Logic as well as the normal functions of the PLB.

5. (original) A method for enhancing the flexibility of Cascade Logic functions in the Programmable logic Block (PLB) of a Programmable Logic Device (PLD), comprising the steps of:

- providing a 2-input selection multiplexer for receiving one input from the output of the Cascade Logic block and the other from the output of the LUT and selecting either the Cascade Logic output or the LUT output as the unregistered output, and
- providing simultaneous access to the cascade logic output and the unregistered output as separate outputs of the PLB for use as sub functions in cascade logic or in other logic functions.

6. (currently amended) The [[A]] method as claimed in claim 5, further including the steps of:

- providing a flip flop connected to the output of the selection multiplexer for providing registered output, and
- providing a 2-input output multiplexer for selecting either the unregistered output or the registered output as the final output of the PLB.

7. (currently amended) The [[A]] method as claimed in claim 5 further including the step of providing an arrangement for feedback of the final output to the input of the LUT to enhance the flexibility of the Cascade Logic as well as the normal functions of the PLB.

8. (original) A method as claimed in claim 5, further including a 2-input Cascade input multiplexer for selecting the Cascade-In signal in either its inverted or non-inverted form as one input to the Cascade Logic.

9. (original) A programmable logic block, comprising:

a logic array operable to generate a first signal;

a first cascade logic circuit coupled to the array and operable to receive a second signal from a second cascade logic circuit of another programmable logic block and to generate a third signal from the first and second signals; and

a first multiplexer operable to receive the first and third signals and a first control signal and to pass either the first or third signal in response to the control signal.

10. (original) The programmable logic block of claim 9 wherein the logic array comprises a look-up table.

11. (original) The programmable logic block of claim 9 wherein the first cascade logic circuit comprises a logic gate.

12. (original) The programmable logic block of claim 9, further comprising a flip flop that is operable to receive the signal passed by the multiplexer.

13. (original) The programmable logic block of claim 9, further comprising:

a flip flop operable to receive the signal passed by the first multiplexer and to generate a flip-flop output signal from the received signal; and

a second multiplexer operable to receive the signal passed by the first multiplexer, the flip flop-flop output signal, and a second control signal, and to pass either the signal from the first multiplexer or the flip-flop output signal in response to the second control signal.

14. (original) The programmable logic block of claim 9, further comprising:

a flip flop operable to receive the signal passed by the first multiplexer and to generate a flip-flop output signal from the received signal;

a second multiplexer operable to receive the signal passed by the first multiplexer, the flip flop-flop output signal, and a second control signal and to pass either the signal from the first multiplexer or the flip-flop output signal in response to the second control signal; and

wherein the logic array is operable to receive the signal passed by the second multiplexer.

15. (original) The programmable logic block of claim 9, further comprising a second multiplexer coupled between the first cascade logic circuit and the second cascade logic

circuit and operable to receive the second signal, a complement of the second signal, and a second control signal and to pass to the first cascade logic circuit either the second signal or the complement of the second signal in response to the second control signal.

16. (original) The programmable logic block of claim 9, further comprising:

an output node; and

wherein the first multiplexer is operable to pass the first or third signal to the output node.

17. (original) An integrated circuit, comprising:

a first programmable logic block having a first cascade logic circuit operable to generate a first signal; and

a second programmable logic block comprising,

a logic array operable to generate a second signal,

a second cascade logic circuit coupled to the first programmable logic block and to the logic array and operable to generate a third signal from the first and second signals, and

a multiplexer operable to receive the second and third signals and a control signal and to pass either the second or third signal in response to the control signal.

18. (original) An electronic system, comprising:

an integrated circuit, comprising,

a first programmable logic block having a first cascade logic circuit operable to generate a first signal, and

a second programmable logic block comprising,

a logic array operable to generate a second signal,

a second cascade logic circuit coupled to the first programmable logic block and to the logic array and operable to generate a third signal from the first and second signals, and

a multiplexer operable to receive the second and third signals and a control signal and to pass either the second or third signal in response to the control signal.

19. (original) The electronic system of claim 18 wherein the integrated circuit comprises a programmable logic device.

20. (original) The electronic system of claim 18 wherein the integrated circuit comprises a field-programmable gate array.

21. (original) A method, comprising:

generating a first signal with a first cascade logic circuit of a first programmable logic block;

generating a second signal with a logic array of a second programmable logic block;

generating from the first and second signals a third signal with a second cascade logic circuit of the second programmable logic block; and

selectively passing either the second or third signal to an output node of the second programmable logic block.

22. (original) The method of claim 21 wherein selectively passing the second or third signal comprises passing either the second or third signal to the output node in response to a control signal.

23. (original) A method, comprising:

generating a first signal with a first cascade logic circuit of a first programmable logic block;

passing a second signal that is selectively equal to either the first signal or a complement of the first signal to a second cascade logic circuit of a second programmable logic block;

generating a third signal with a logic array of the second programmable logic block;

generating from the second and third signals a fourth signal with the second cascade logic circuit; and

selectively passing either the third or fourth signal to an output node of the second programmable logic block.

24. (original) The method of claim 23 wherein passing the second signal comprises setting the second signal equal to either the first signal or a complement of the first signal in response to a control signal.

25. (original) A method, comprising:

generating a first signal with a first cascade logic circuit of a first programmable logic block;

generating a second signal with a logic array of a second programmable logic block;

generating from the first and second signals a third signal with a second cascade logic circuit of the second programmable logic block;

selectively passing either the second or third signal; and

registering the passed signal.

26. (original) The method of claim 25, further comprising selectively passing the passed signal or the registered signal to an output node of the second programmable logic block.

27. (original) The method of claim 25, further comprising selectively feeding back the passed signal or the registered signal to the logic array.